Upscaling of Perovskite/*c*-Si Tandem Solar Cells by Using Industrial Adaptable Processes

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Abstract. The perovskite material has been introduced as a novel type of wide-bandgap (WBG) light absorber in photovoltaics. Recently, perovskite/crystalline silicon (*c*-Si) tandem solar cells have achieved efficiencies beyond those of the silicon single-junction limit, which makes them very promising as a next-generation solar cell technology to further increase conversion efficiency. However, most of the efficiency-record tandem cell devices are those with laboratory-relevant architectures, e.g., a small active area (≤ 1cm^2) on ~250 µm thick Float-Zone (FZ) Si bottom cells and with evaporated metallization. Scaling-up of perovskite/*c*-Si lab tandem solar cells with industrial adaptable processes is needed to accelerate the time-to-market. In this work, we integrate the industrial compatible process for two-terminal perovskite/*c*-Si tandem solar cells, which includes the combinations of "screen-printed silver (SP-Ag) grids and transparent conductive oxides (TCOs)" front-electrode setup; and large area slot-die coated (SDC) WBG perovskite layer on the Czochralski (Cz) *c*-Si bottom cells. It is demonstrated that SP-Ag with a low thermal budget (150 °C) curing can achieve a grid resistance of 1.6 Ω/cm on and metal-to-TCO contact resistivity of 2 mΩ·cm^2. The SDC perovskite layer exhibits good homogeneity in thickness and crystallization. There was no further degradation after the additional post-printing curing step, indicating good thermal stability. Under AM 1.5G irradiation, the champion 4 cm^2 perovskite/*c*-Si tandem solar cells have a stabilized power conversion efficiency (PCE) of 24%.

Keywords: perovskite, upscaling, industrial, slot-die coating, Cz-Si wafer, tandem solar cells, screen-printed, triple-halide

INTRODUCTION

Solar is crowned "king of the world's electricity markets" in the new IEA report.[1] Based on today's policy settings; it is on track to set new records for deployment every year after 2022. Since 2010, the cost of energy has dropped by 82% for solar photovoltaic (PV)[2]. One way to further continue this trend is to increase cell/module efficiency, which has a direct effect on lowering the levelized cost of electricity (LCOE)[3]. As crystalline silicon (*c*-Si) single-junction solar cells are approaching their practical physical performance limit in the industry[4], numerous research groups and industrial companies are now looking for a promising solution to push efficiencies beyond the limit of *c*-Si single-junction solar cells. For this intention, better utilization of the solar illumination spectrum is required, which can be realized with multi-junction solar cells. Two is the simplest number of multi-junction but with the highest relative efficient gain[5], which is fabricated by stacking a wide-bandgap (WBG) top cell on top of a narrow-bandgap bottom cell. The sub-cells are electrically connected in series with two terminals, only the lowest current mismatch can bring

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the best performance. The top cell with a bandgap of 1.72 eV is optimum to pair with the silicon (Si) bottom cell (1.12 eV bandgap)[6]. Recently, in the laboratory, two-terminal (2T) metal-halide perovskite/*c*-Si tandem solar cells have achieved efficiencies above 29% and beyond the silicon single-junction limit[7], which demonstrates the realization of this high-efficiency tandem technology. Scaling-up of perovskite/*c*-Si lab tandem solar cells with industrial adaptable processes is needed to accelerate the time-to-market. In this work, we demonstrate the challenges of upscaling, which include: (1) optimization of the "screen-printed silver (SP-Ag) grid and DC sputtered transparent conductive oxide (TCO)" front electrode; (2) the challenge of integrating the front-electrode setup into the perovskite/*c*-Si tandem devices; (3) the homogeneity and thermal stability of the slot-die coated (SDC) WBG large-area perovskite layer on the Cz-Si bottom cell. Finally, with these processes, we demonstrate a 4 cm^2 area perovskite/*c*-Si tandem solar cell that achieves a power conversion efficiency of 24.1%.

EXPERIMENTAL

Materials and Preparation for Perovskite Precursor Solution

As precursor materials, we used anhydrous DMF (dimethylformamide), NMP (1-Methyl-2-pyrrolidinone), and LiF (lithium fluoride) purchased from Sigma Aldrich, C_{60} (sublimed) from CreaPhys GmbH, and MACl (methylammonium chloride) from Greatcell Solar. FAI (formamidinium iodide) was purchased from Dyenamo. CsI was purchased from abcr GmbH. PbI_2 (lead iodide), $PbBr_2$ (lead bromide) and $PbCl_2$ (lead chloride) were bought from TCI. The triple-halide perovskite was $Cs_{0.22}FA_{0.78}Pb(I_{0.85}Br_{0.15})_3$ (1 mol, referred to Cs22Br15) + 5 mol % $MAPbCl_3$, which means for each mol Cs22Br15, with additional 5 mol % $MAPbCl_3$ was added to form the "triple-halide" perovskite salt. The solvent volume is the sum of the amounts of DMF and NMP (13.3:1, v/v). To simplify the concentration calculation, the volume expansion was ignored. In this work, a 1.4 M precursor solution was prepared.

Perovskite Film Fabrication

The wet perovskite film coating was performed at 21 °C by using a commercial slot-die coater from FOM Technologies (FOM alphaSC) equipped with a 10 cm wide slot-die head. The distance between the slot-die head and the substrate was fixed at 300 µm and the coating speed was 5 mm/s with a pump rate of 10 µl/s. A quenching step follows, where a nitrogen flow (30 psi) is passed through an air knife (Nex Flow, 10012XHA) with a 7.5 mm/s drying speed to the coated wet film to control the nucleation and crystal growth of the perovskite layer. Afterward, an annealing step (150 °C/20 min on a hot plate) was performed to crystallize the perovskite film. All the above steps are processed in a glove box with a controlled N_2 atmosphere with H_2O and O_2 levels below 10 ppm.

Bottom Cells (*c*-Si Solar Cells) Fabrication

Industrial-type rear-junction SHJ cells based on Cz-Si *n*-type wafers with a chemically polished front and a random-pyramid rear side were used as bottom cells, featuring a 100-nm thick *n*-doped nanocrystalline silicon oxide layer ((*n*)-*nc*-SiO_x:H) on the front side. Both the front (20 nm) and the rear (150 nm) transparent conducting oxide (TCO) layers were DC sputtered (A600V7 from Leybold Optics) from a commercial (Advanced Nano Products) In_2O_3-based TCO target ("new SCOT") at room temperature. A 400 nm thick layer was sputtered on the textured side as a rear electrode. Both contact-layer stacks (TCO and Ag layers) were deposited using aligned shadow masks with an opening of 2.13 x 2.13 cm^2. After fabrication, the bottom cells were annealed at 210 °C for 10 min before the top layers deposition.

Perovskite/*c*-Si Tandem Solar Cells Fabrication

The Si bottom cell's front surface was blown clean with N_2 and activated by UV-O_3 treatment (UVOH 150 Lab, FHR) for 15 min. The tandem cell schematic cross-section and process flow are shown in Fig. 1(a) and Fig. 1(b), respectively. A SAM (self-assembled monolayer) solution was prepared from 2PACz ([2-(9*H*-Carbazol-9-yl)ethyl]phosphonic acid, synthesized by TCI) dissolved in absolute ethanol (0.3 mg/ml) and deposited by spin coating, followed by 100 °C heating for 10 minutes, to form a hole-transport-layer (HTL). The spin-coated SAM layer and slot-die coated perovskite layer deposition steps were conducted in a nitrogen atmosphere. As shown in Fig. 2(a),

a 1-nm thick LiF interlayer was evaporated at a rate of 0.05 Å/s between perovskite and C_{60}. Afterward, without breaking the vacuum, 23 nm of C_{60} was thermally evaporated at a rate of 0.15 Å/s onto the perovskite film. 20 nm SnO_2 was deposited using a thermal ALD (atomic layer deposition) reactor (GEMStar from Arradiance). Subsequently, a 40-nm thick In_2O_3-based TCO layer was deposited using the same DC sputtering tool and shadow mask mentioned in the previous section. Afterward, front metal contacts were formed by screen printing using Ag pastes developed by Toyal for low-temperature curing. The curing was done at 150 °C for 20 minutes in N_2 on a hotplate. Finally, 100 nm LiF was thermally evaporated as an antireflective coating. The designated cell area was 4 cm² as defined by a shadow mask during the *J-V* measurement.

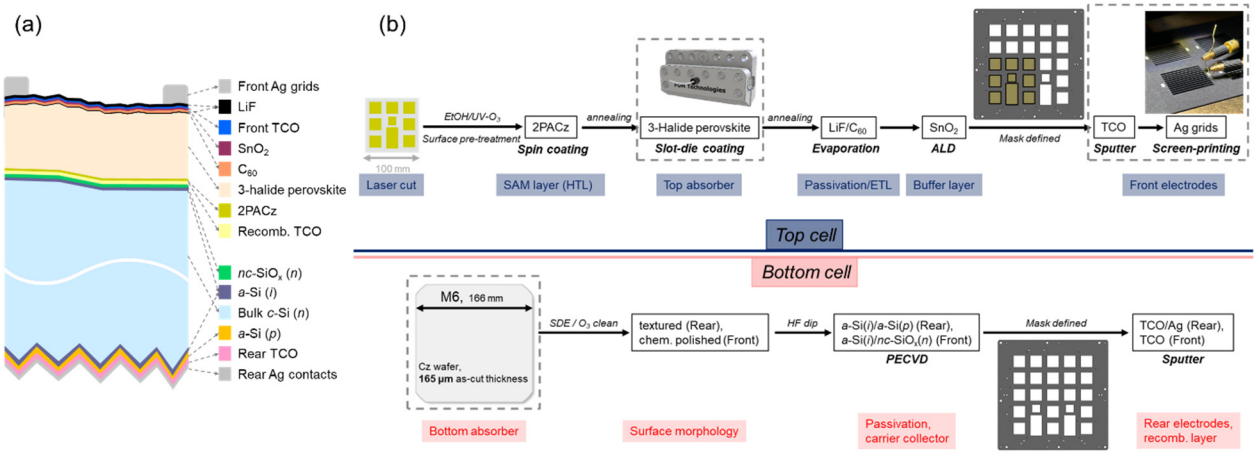

FIGURE 1. (a) Schematic cross-sectional structure and (b) process flow of the perovskite/*c*-Si tandem solar cells.

Characterization

For fabricating Ag/TCO contact resistivity test devices, we used commercial *n*-type Cz silicon wafers. After saw damage etching, a 60 nm SiO_xN_y is deposited as an insulation layer. Subsequently, 40 nm thick In_2O_3-based transparent conductive oxide (TCO) layers were deposited with various parameters with the same sputter tool from a tube target. Afterward, we used screen printing with an Ag paste developed for low-temperature curing to print transfer-length-method (TLM) test patterns and finger grids. Curing was done at 150 °C for 20 minutes in the air on a hotplate for extracting the contact resistivity (ρ_c) and grid resistance (R_{grid}). Photoluminescence (PL) measurement samples are manufactured by using the slot-die coating machine to form the triple-halide WBG (1.68 eV nominal value) perovskite ($Cs_{0.22}FA_{0.78}Pb(I_{0.85}Br_{0.15})_3$ + $(MAPbCl_3)_{0.05}$) wet film (100 cm²) on the chemical polished Cz-Si wafer with 20 nm TCO/hole transportation layer (2PACz). After crystallized perovskite film is formed, the sample is measured with steady-state PL before and after an additional curing step (150 °C/20 mins in the N_2). The integration time is 2s with 470 nm excitation light sources. X-ray diffraction patterns (XRD) were measured using a Bruker D8 diffractometer in Bragg-Brentano geometry with a custom-made inert sample holder at room temperature. For all measurements, the Cu K-alpha radiation emitted from an X-ray tube operated at 40 mA and a 40 kV acceleration voltage was used. Scanning electron microscopy (SEM) (Hitachi S4100) is applied to observe the cross-sectional microstructure of the perovskite layer thickness.

The tandem solar cells were measured in the air under AM1.5G (1 sun) equivalent illumination with a Wavelabs Sinus-70 LED class AAA sun simulator. The backside of the cell was contacted with a metal vacuum chuck at 25 °C, whereas the front side was contacted with two Au probes. A black laser-cut aperture mask covered the substrate outside of the active area. The *J-V* measurements and maximum power point (MPP) tracks were recorded using a home-built LabView software. The external quantum efficiency (EQE) was recorded with Enlitech QE-R using chopped (79 Hz) monochromatic light from a Xe and He lamp, respectively. For reflection measurements, a PerkinElmer Lambda-1050 UV/VIS/NIR spectrophotometer with an integrating sphere was used.

RESULTS AND DISCUSSION

Why The Grids Are Necessary

Transparency of the front TCO layer can be improved by reducing the thickness or carrier concentration. However, this will increase the TCO sheet resistance (R_{sheet}), thereby, the power loss induced by lateral carrier transportation before being collected at the metal fingers. Figure 2(a) depicts the impact of varied R_{sheet} and grid pitch on J_{mpp} simulated by Quokka3[8], which is under the assumption of 18 mA/cm^2 J_{SC} (for the devices with a front flat surface, without an additional ARC layer). The black color line represents a device without grids, when R_{sheet} increases from 45 Ω/sq (the present value for small area devices), the FF and hence J_{mpp} drops sharply. The 0.2-0.3 mA/cm^2 J_{SC} losses induced by 1.6-2.4% grid shading area ratio can be easily compensated by reducing the thickness of TCO. Applying the grids facilitates more device design freedom.

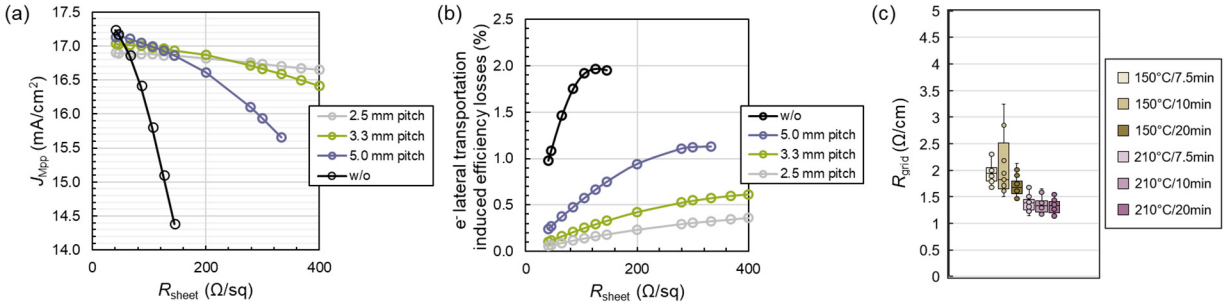

FIGURE 2. The Quokka3 simulated impact of varying $R_{sheet,\ TCO}$ and grid pitch on (a) the J_{mpp} losses and (b) the efficiency losses induced by carrier lateral transportation. (c) The screen-printed Ag grid resistance with different curing thermal budgets. The input grid width is 60 μm.

SP-Ag Grid Resistance with Low Curing Thermal Budget

The challenge of adapting SP-Ag grids on the perovskite/*c*-Si tandem solar cells is highly related to the thermal budget for post-printing curing, which can be divided into three parts. In the first part, we discuss grid resistance; Fig. 2(c) shows the R_{grid} of commercial low-temperature curing SP-Ag paste with varying thermal budgets. Compared with the typical 210 °C curing temperature used for SHJ solar cells[9], the R_{grid} cured at 150 °C just increases a bit with respect to 210 °C curings, from 1.0-1.5 to 2.0-2.5 Ω/cm, depending on the curing time. The efficiency loss caused by this R_{grid} range is less than 0.01% which is shown in the black color block of Fig. 3(b). This can be attributed to the current match of the 2T perovskite/*c*-Si tandem solar cells, making J_{SC} much lower (almost half) than the silicon single-junction solar cells.

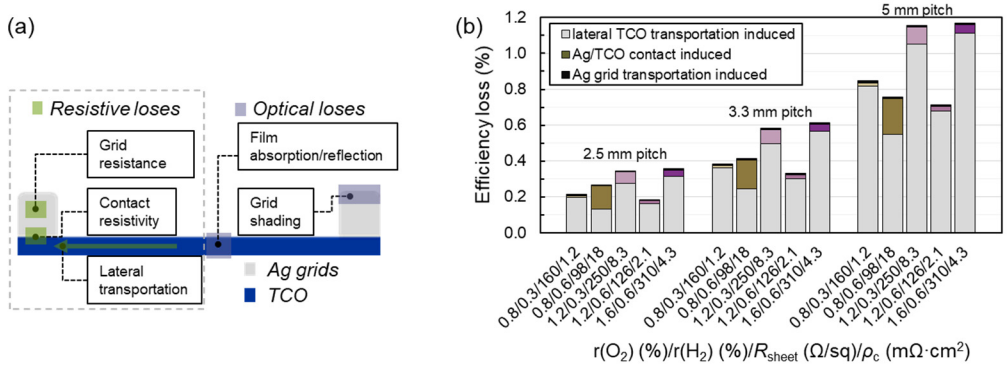

FIGURE 3. (a) Schematic representation of resistive and optical losses in "Ag grids + TCO" front-electrodes. (b) Efficiency losses induced by the carrier transport in the front electrodes simulated by Quokka3 for different TCO and grid processes and properties: r(O_2) and r(H_2) mean O_2/(Ar + O_2) and H_2/(Ar + H_2) flow ratio during TCO sputtering, sheets resistance of the TCO and TCO/grid contact resistivity.

Contact Resistivity of SP-Ag/TCO with Low Curing Thermal Budget

The second part of the challenge is the contact resistivity (ρ_c) of -SP-Ag grid/TCO- with a lower curing thermal budget. Nowadays, the state-of-the-art ρ_c both on commercial SP-Ag *p*-PERC (high sintering thermal budget)[10] or SHJ (low sintering thermal budget)[11] solar cells are below 1 mΩ·cm^2. In Fig. 4(a) we varied the gas flow ratios r(O_2) and r(H_2) during the TCO sputtering process, to obtain different carrier concentrations and either amorphous or crystallized TCO layers, which helps to optimize the ρ_c under curing in the air at 150 °C for 20 minutes. We suppose that the lower r(O_2) (0 and 0.8%) leads to a TCO growth with a higher amorphous fraction, which can be proven by a broad XRD peak center at 2θ = 30.6° (green lines in Fig 4(b)). Meanwhile, increasing r(H_2) to 0.6%, there is only a small (222) peak at around 2θ = 30.6° indicating the presence of a few small crystallites inside the amorphous matrix. This surface arrangement tends to form a lower ρ_c to the Ag finger after curing (around 1-5 mΩ·cm^2, shown in Fig. 4(a)). For the higher r(O_2) (1.2 and 1.6%), the ρ_c is dominated by the carrier concentration (n_c), the higher the n_c (high hydrogen doped), the lower ρ_c. The films show a strong (222) peak around 2θ = 30.6° (purple lines in Fig 4(b)), which can be assigned to cubic bixbyite indium oxide[12], In_2O_3. Furthermore, increasing from 0 to 0.6% under high r(O_2) condition, an additional peak appears at 2θ = 31.6°, which reveals the (220) planes of cubic indium hydroxide[12], $In(OH)_3$.

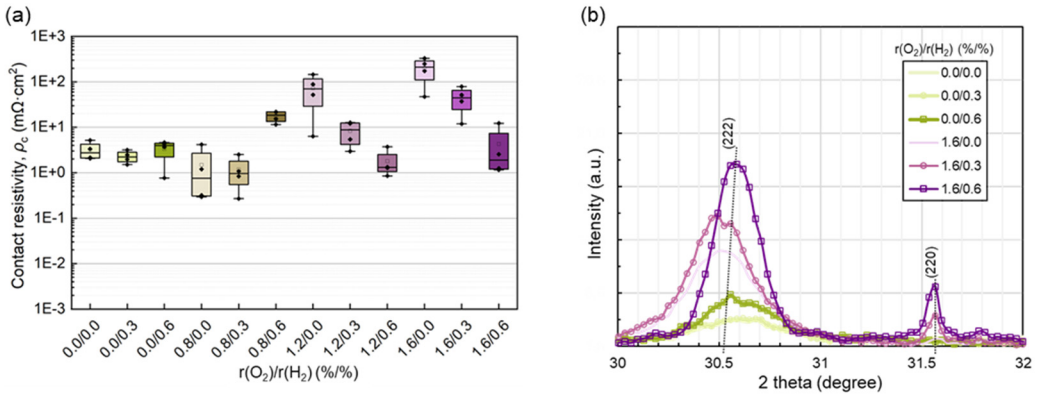

FIGURE 4. (a) The contact resistivity (ρ_c) of SP-Ag grid /TCO interface, extracted by TLM measurement. (b) X-ray diffraction (XRD) patterns of hydrogen doped indium oxide-based TCO films sputtered under different r(O_2) and r(H_2) conditions and annealed in air at 150 °C for 20 min.

Considering together with the R_{grid} and grid shading, the efficiency losses with five different r(O_2)/r(H_2) flow ratios during deposition and their corresponding R_{sheet} and ρ_c are simulated and shown in Fig. 3(b). The highest resistance-induced efficiency loss comes from the R_{sheet}, not from the R_{grid} nor the ρ_c, which again emphasizes the necessity of adding the grids when scaling up the device area. When the grid pitch is reduced from 5 to 2.5 mm, even if the R_{sheet} is as high as 300 Ω, the efficiency loss can be suppressed to about 0.3% (the grey lines in Fig 2(b)). In the same situation as the R_{grid} induced efficiency loss, due to the low J_{SC} condition of the tandem solar cells, it has better tolerance to the high ρ_c. For example, as shown in Fig. 3(b), the efficiency loss is less than 0.05% when ρ_c is lower than 10 mΩ·cm^2.

Large Area Homogeneity and Thermal Stability of The Slot-Die Coated Perovskite Films

Industrial adaptable perovskite deposition methods, such as spray coating[13], blade coating[14], and slot-die coating[15] have recently been proposed. Compared to spin-coating employing anti-solvent quenching to produce high-quality films, the slot-die coating requires carefully designed perovskite ink solution systems and corresponding quenching methods. In this work, we made use of N_2 and an air knife to perform gas quenching, and the detailed process parameters are given in the experimental section. Slot-die coating is a solution process, which is promising to scale up perovskite film deposition. Due to the perovskite/c-Si tandem solar cell application, the demand for WBG perovskite has increased for utilizing top cell compositions with optimal photocurrent match. The incorporation of chloride increases the bandgap of triple-halide perovskite up to 1.68 eV and low methylammonium (MA) concentration improves the thermal stability at higher temperatures[16].

In this work, we emphasized three main challenges when upscaling perovskite/*c*-Si tandem solar cells:

1. The Si bottom cell front surface morphology should be carefully processed and monitored. Commercial Cz-Si wafers were used in this work. After the saw damage etching step, a chemically polished surface with (100) orientation was prepared for the perovskite ink coating. Compared to the mechanically polished FZ wafer surface, the chemically polished Cz-Si has a rougher surface. Figure 5(a) shows the SEM cross-sectional image of a slot-die coated perovskite film with a film thickness over 1 µm grown conformally on a 1 µm step height/15° slope angle chemical-polished surface. If the slope angle is too high, the perovskite film is difficult to completely cover the Si surface, and it is easy to cause shunting.
2. Controlling the crystallization of the triple-halide perovskite material and obtaining uniform perovskite layers with the desired thickness. The crystal properties can be further investigated by XRD measurements. Figure 5(b) shows the characteristic perovskite 2θ peak at 14.1°, revealing the ordered crystal structure of ABX_3. We monitored 4 points on the 9 x 9 cm^2 slot-die coated area with identical characteristic peaks, demonstrating the crystallographic homogeneity of the larger area perovskite films. The EQE measurements in Fig. 5(c) show the characteristic absorption of the top cell. It can absorb photons with a wavelength less than 740 nm, which represents a wide bandgap of 1.68 eV (where the blue dashed arrow points to). The EQE in the 600–700 nm wavelength range is determined by the thickness of the perovskite films, with thicker layers enhancing photon harvesting. Because the absorption coefficient is much lower near the bandgap wavelength. This is an alternative (non-destructive) method to monitor film thickness other than measuring it from SEM cross-sectional images. The uniformity of film thickness is well demonstrated by the EQE curves and the standard deviation of 0.23 mA/cm^2 of the J_{SC} at eight positions. For the larger area, SDC perovskite films in this work, good uniformities are exhibited in both crystal properties and film thickness.

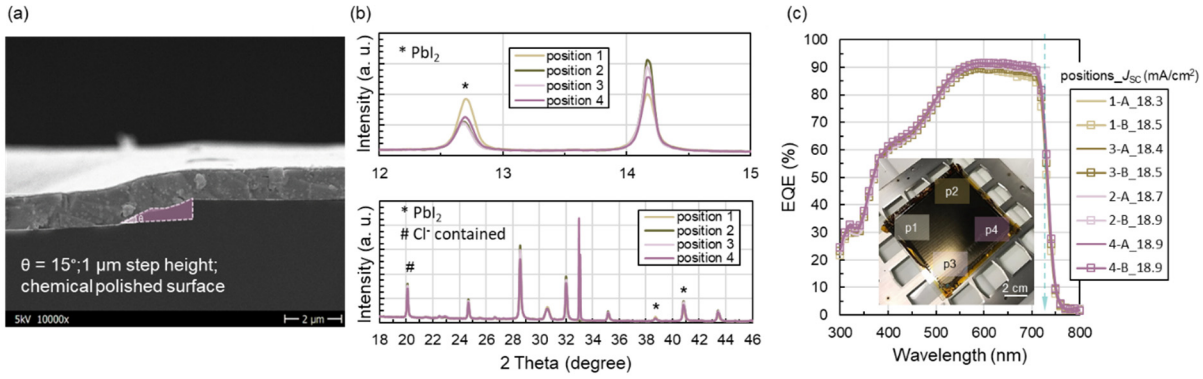

FIGURE 5. (a) Cross-sectional SEM images and (b) X-ray diffraction patterns of the slot die coated triple-halide perovskite layers (9x9 cm^2) deposited on 2PACz/TCO/(SHJ) bottom cell after 150 °C for 20 min annealing in N_2 atmosphere. (c) the EQE measurements and the integrated (300-800 nm) J_{SC} of the perovskite top cell. The corresponding positions are noted on the appended image.

3. The challenge of integrating the SP-Ag + TCO contact with the perovskite film is due to the low thermal stability of the perovskite cell, as most of the state-of-the-art metal-halide perovskite films will degrade when annealed above 110 °C. However, such a temperature is challenging to form a high-quality front-electrode setup (with low R_{grid} and ρ_c), and after silver paste printing tests, at least 150 °C was required to minimize resistive losses and needed to crystallize the TCO layer. To investigate the impact of the additional curing step (post-printing curing) on the thermal stability of slot-die coated triple-halide perovskite film, we applied PL to measure the film with an area of 100 cm^2 before and after an additional 150 °C curing for 20 minutes in N_2 (excluding the impact of humidity and O_2). Figure 6(a) shows the average peak emission remains at the same energy (1.67 eV), which implies the composition (bandgap) of triple-halide perovskite has not changed by the additional annealing. On average, no significant enhancement of thermally induced defects in the film after additional curing is found, which can be monitored from similar PL quantum yield (PLQY) and quasi-Fermi level splitting (QFLS) values derived from the PL spectra (Fig. 6(b) and (c)).

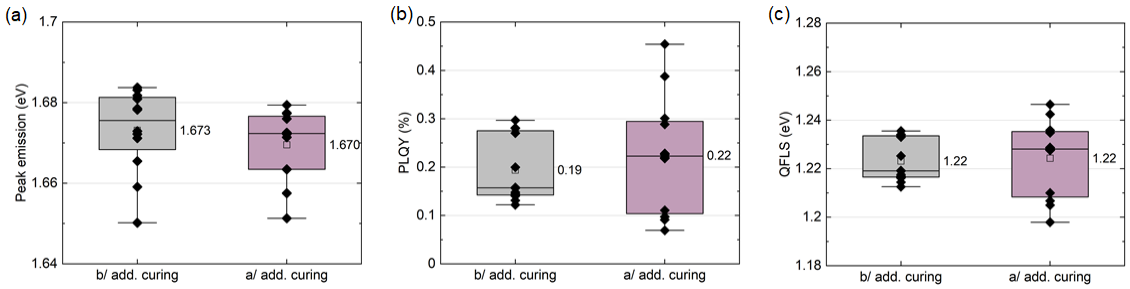

FIGURE 6. PL spectral measurements of 100cm^2 test device (Si/TCO/2PACz/perovskite) to extract: (a) Peak emission energy; (b) PL quantum yield (PLQY) and (c) quasi-Fermi level splitting (QFLS). The left grey box is before, and the right purple box is after additional curing.

Performance of 2T Perovskite/*c*-Si Tandem device

We fabricated monolithic tandem solar cell devices based on the optimized processes as described in the previous sections. The process flow is summarized in Fig. 1(b). The cells are built on commercial type Cz-Si based SHJ cells, slot-die coated 1.68 eV WBG perovskite layers, and a front-electrode setup consisting of DC sputtered indium oxide-based TCO with ($r(O_2)/r(H_2)$ = 1.2%/0.6%) sputtering gas flow ratio, and a screen-printed Ag grid. For minimizing the resistive loss for the Ag grids, the 150 °C/20 min thermal budget is chosen for the post-printing curing. In Fig. 7(a), we demonstrate the *J-V* characteristics of the tandem solar cell (area 4 cm^2), which shows a high V_{OC} (1.9 V) and almost no hysteresis between the forward and reverse *J-V* scan. The corresponding stabilized PCE (Fig. 7(c)) after 300s MPP tracking is 24%. Figure 7(b) shows the EQE spectrum of the champion device. It reveals almost no current mismatch. We suggest that a too low reflective index of the (*n*)-*nc*-SiO_x:H optical interlayer (i.e., too oxidic) leads to increased reflection and reduced absorption in the near-infrared, hence reducing the photocurrent in the Si bottom cell[17]. Therefore, we reduced the perovskite thickness to 750 nm to allow more photons with wavelengths of 600-740 nm to penetrate and be absorbed in the bottom cell, thus minimizing the current mismatch. One possible cause of the low FF of the devices could also be induced by a too oxidic interlayer, forming a poor contact with the TCO interlayer[18,19]. Figure 7(d) shows the FF analysis under the sub-cell current limiting conditions[20]. Although the FF usually is limited by the perovskite top cell, the low FF of 73.8% under the bottom cell current limiting condition might correspond to our above interlayer hypothesis. Further characterization and optimization are needed.

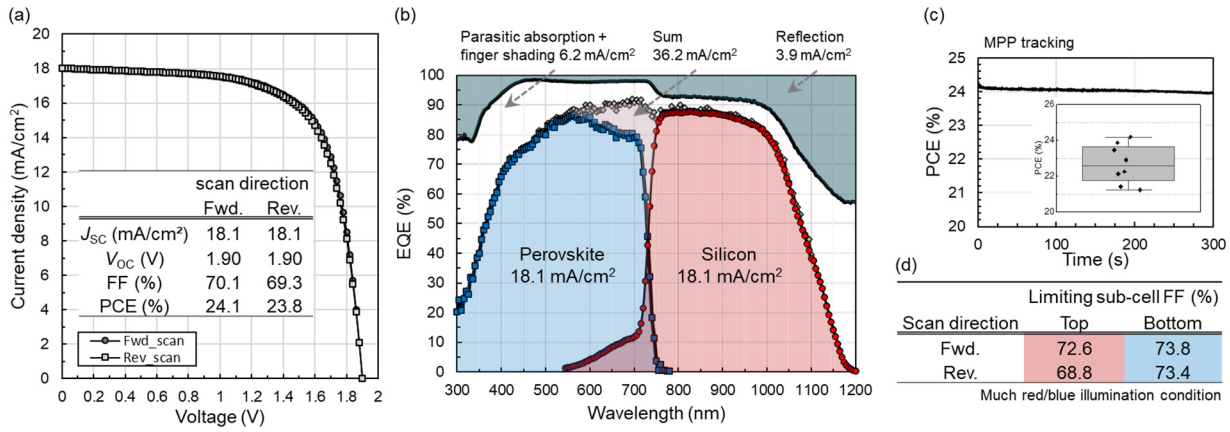

FIGURE 7. Performance of the champion SDC perovskite/SHJ tandem solar cells. (a) In-house measured current-voltage (*J-V*) curve of the champion tandem device (4 cm^2) with power conversion efficiency (PCE) of 24.1% under standard test conditions. (b) EQE and 1-reflectance curves of the champion tandem device with SDC perovskite, the around 3.5% Ag grids shading is considered. (c) The 300 seconds MPP tracking. The inset figure shows the statistical distribution of PCE. (d) The limiting sub-cell fill factor (FF) of the tandem solar cell from (a) under the current mismatching condition and in calculated photogeneration (J_{SC} =16 and 18.1 mA/cm^2 for top and bottom cell limiting conditions, respectively)

CONCLUSIONS AND OUTLOOK

In this work, we have demonstrated tandem cells integrating industrial adaptable process steps by applying a front-electrode consisting of screen-printed Ag grids and in-line DC sputtered TCO, and deposition of slot-die coated perovskite on Cz-Si based SHJ bottom cells. The front TCO sputter process was optimized for achieving a low TCO/metal contact resistivity of 2 mΩcm^2. The 150 °C/20 min thermal budget for post-printing curing helps to minimize the R_{grid} lower than 2 Ω/cm, and this additional curing step has almost no degradation (checked from the XRD and PL measurement) on the triple-halide WBG perovskite layer. Taken together, the SEM, XRD, and EQE observations show the large area slot-die coated perovskite layer exhibits good homogeneity both in thickness and crystallization properties. The champion tandem solar cell reaches a PCE of 24% (MPP tracked) with a high V_{OC} of 1.90 V on a 4 cm^2 device area. While a J_{SC} of 18.5 mA/cm^2 is promising, the FF of our device still needs improvement. In addition to the suggested poor internal contact induced by the *nc*-SiO_x:H layer, the low FF most likely is limited by the triple-halide perovskite, which we are supposed to be induced by the excess PbI_2 accumulated[21] at the interface of perovskite and C_{60}. If we assume a slightly improved J_{SC} and solve these FF limitations while keeping the V_{OC} of 1.9 V, this will result in an efficiency well above 26%, paving the way for industrial, full-wafer tandem cells by slot-die coating.

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